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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ROBERT E. CYPHER

Appeal 2009-004226
Application 10/813,857
Technology Center 2100

Decided: March 15, 2010

Before JOHN A. JEFFERY, LEE E. BARRETT, and JOSEPH L. DIXON, *Administrative Patent Judges*.

JEFFERY, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant appeals under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1-48. We have jurisdiction under 35 U.S.C. § 6(b). We reverse.

STATEMENT OF THE CASE

Appellant invented a shared memory multiprocessing system that includes nodes. The nodes are configured: (1) to maintain an indication whether to respond to address packet request to access a coherency unit (e.g., a cache line) and (2) to store a node identifier for the coherency unit. *See generally* Spec. ¶¶ 0001, 0011, and 0069.

Claim 1 is reproduced below with the key disputed limitations emphasized:

1. A system, comprising:

a plurality of nodes coupled by an inter-node network, wherein each node includes a plurality of active devices, a memory subsystem, and an address network and a data network respectively configured to convey address packets and data packets between the plurality of active devices and the memory subsystem;

wherein a memory subsystem included in a node of the plurality of nodes is configured to maintain a response indication indicating whether the memory subsystem should send a data packet corresponding to a coherency unit in response to receiving from an active device in the node an address packet requesting an access right to the coherency unit;

wherein the node is configured to store a node identifier for the coherency unit, *wherein the node identifier identifies a different node of the plurality nodes in which the coherency unit is in a modified global access state.*

The Examiner relies on the following as evidence of unpatentability:

Liencres	US 5,434,993	July 18, 1995

THE REJECTION

The Examiner rejected claims 1-48 under 35 U.S.C. § 102(b) as anticipated by Liencres. Ans. 3-11.[1]

Regarding independent claim 1, the Examiner finds that Liencres discloses all the limitations in claim 1, including the disclosed status bits reading on the limitation "the node identifier identifies a different node of the plurality nodes in which the coherency unit is in a modified global access state." Ans. 3-4.

Appellant contends, among other arguments, that Liencres does not disclose a node configured to store a node identifier that identifies a different node from the nodes in which the coherency unit is in a modified global access state. App. Br. 5-7. In Appellant's view, Liencres' status bits for each cache line only show a valid, shared, and owned status. App. Br. 6-7; Reply Br. 5.

The issue before us, then, is as follows:

ISSUE

Under § 102, has the Examiner erred in rejecting claim 1 by finding that Liencres discloses a node configured to store a node identifier that "identifies a different node of a plurality of nodes in which the coherency unit is in a modified global access state"?

[1] Throughout this opinion, we refer to (1) the Appeal Brief filed January 21, 2008; (2) the Examiner's Answer mailed March 25, 2008; and (3) the Reply Brief filed May 27, 2008.

FINDINGS OF FACT

1. The Specification states "a 'coherency unit' is a number of contiguous bytes of memory that are treated as a unit for coherency purposes . . . . In some embodiments, the coherency unit may be a cache line or a cache block." Spec. ¶ 0069.

2. The Specification defines "global access state" as "the access rights associated with a particular coherency unit within a particular node. For example, in some embodiments, the global access states may be . . . Modified (maximum access right = write access). If a coherency unit is in the Modified global access state in a particular node, one of the devices within that node may have a write access right to that coherency unit." ¶ 00182.

3. Liencres discloses a multiprocessor system with processor subsystems 20 having a bus cache controller 31, a cache bus 33, and a processor module 32. The memory bus 25 couples the main memory 23 to the processor subsystems 20. Col. 6, ll. 1-50; Fig. 3a.

4. Liencres discloses the processor module 32 includes a processor 21, a processor cache controller 35, and cache memory 37. The processor cache controller 35 maintains a cache directory 34 containing address tags and status bits for the cache lines stored in processor cache memory 37. Col. 6, ll. 62–67 and col. 9, ll. 14-16; Fig. 3a.

5. Liencres discloses the bus cache controller 31 maintains a cache directory 46 also containing the address tags and status bits for data in cache directory 37. Col. 7, ll. 3-19; Fig. 3a.

6. Liencres discloses in the Background of the Invention section that common status bits maintained in cache directories include "valid," "shared," and "owned." The "valid" bit reflects whether the information stored in the cache line is currently valid. The "shared" status bit indicates whether the information in the cache line is shared by other cache memories. The "owned" status bit indicates that the information in the cache line has been modified without being written back to the main memory. A "shared" cache line cannot be modified without first invalidating the cache line in the other cache memories. Col. 1, l. 61 – col. 2, l. 12.

7. Liencres discloses, when a cache memory system for a processor subsystem "owns" a cache line, the processor is allowed to modify the contents of the cache line. Col. 7, ll. 46-48; Fig. 1b.

8. When the memory request by processor 21 cannot be fulfilled by data in processor cache memory 37, Liencres discloses processor cache controller 35 sends to a read request to bus cache controller 31. Controller 31 broadcasts the read request packet across memory bus 25, and the device that contains the requested memory address (e.g., an owned processor subsystem) responds with a read reply packet containing the requested subblock. Col. 7, ll. 22-44.

ANALYSIS

Based on the record before us, we find error in the Examiner's anticipation rejection of claim 1 which calls for, in pertinent part, the node to be configured to store a node identifier that identifies a different node of the nodes in which the coherency unit is in a modified global access state. Liencres discloses a system having processing subsystems or nodes 20.

FF 3. Each of Liencres' nodes 20 has two cache directories (i.e., 34 and 46) containing status bits for a cache line or coherency unit. *See* FF 1, 4, and 5. These disclosed status bits can therefore be "a node identifier for the coherency unit" as recited in claim 1.

Liencres discloses three common status bits: (1) valid; (2) shared; and (3) owned. FF 6. A "valid" status bit reflects the current validity of the information stored in a cache line. *Id.* A "shared" status bit shows whether the information in a cache line is shared by other cache memories. *Id.* Lastly, an "owned" status bit reflects a cache line's information has been modified without being written back to the main memory. *Id.* Liencres also discloses, when a cache memory (e.g., 37) for a processing subsystem (e.g., 20) "owns" a cache line (e.g., has a status bit "owned"), the processor subsystem or node (e.g., 20) can modify the cache line. FF 7. Such a function gives the node (e.g., 20) write access rights associated with a particular coherency unit or identifies the node is in a modified global access state, as described by Appellant. *See* FF 2 and 7.

However, Liencres' cache directories fail to include a node identifier (e.g., a status bit) that identifies a *different* node within the system as claimed. First, Liencres does not state the status bits discussed in the Background of the Invention section necessarily correspond to the status bit types discussed in connection with the Figure 3 embodiment. *See* FF 4-7. Second, Liencres discloses that the status bits in the cache directories 34 and 36 are for the data in the cache memory 37 (*see* FF 4 and 5), or identifies when coherency unit (e.g., a cache line) in the *same* node is in a modified global access state. Liencres, however, is silent about whether the status bits or node identifiers in a node's cache directories identify that a different node

is in a modified global access state. Third, Liencres discloses the node (e.g., 20) can identify when the request by processor 21 cannot be fulfilled by cache memory and requests information across memory bus 25. FF 8. Liencres, nonetheless, broadcasts the request to all devices rather than identify the different node "in which the coherency unit is in a modified global access state" as recited. *See id.*

The Examiner contends that Liencres discloses in Figures 1a and 1b that a node identifier identifies a different node in which the coherency unit is in a modified global access state when a bit is not set "valid" but is marked "shared." Ans. 12-13. We disagree. As stated above, the Background of the Invention section does not necessarily correspond to the other Liencres' embodiments. Thus, this portion in Liencres (FF 6) may not hold true to the Figure 3 embodiment in Liencres. Additionally, Liencres fails to identify which node – let alone a different node – modifies the "shared" cache line or has write access (i.e., a modified global access state (*see* FF 2)) to the cache line. We therefore find that this discussion in Liencres is inadequate to disclose a node is configured to store a node identifier for a coherency unit that identifies a different node has the coherency unit in a modified global access state as recited in claim 1.

Claim 17 recites a similar limitation of a node "configured to store a node identifier for the coherency unit, wherein the node identifier identifies a different node in the multi-node system in which the coherency unit is in a modified global access state." Claim 33 similarly recites a method in which "the node sends a coherency message requesting the access right to a different node of the plurality nodes in response to a node identifier identifying the different node as a node in which the coherency unit is in a

modified global access state." For the reasons discussed above, the Examiner similarly erred in rejecting these claims. Additionally, claims 2-16, 18-32, and 34-48 depend from claims 1, 17, and 33 respectively, and, likewise, we find the Examiner erred in finding Liencres anticipates these claims.

For the foregoing reasons, Appellant has shown the Examiner erred in rejecting claims 1-48. We will therefore not sustain the anticipation rejection of claims 1-48.

CONCLUSION

The Examiner erred in rejecting claims 1-48 under § 102.

ORDER

The Examiner's decision rejecting claims 1-48 is reversed.

REVERSED

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